

Claims

What is claimed is:

- [Handwritten: See A1]*
- [Vertical stamp: RECEIVED]*
- [c1] An apparatus for reducing a magnitude of a rate of current change of an integrated circuit, comprising:
- a control stage that generates a control signal dependent on whether power consumption by the integrated circuit needs to be reduced; and
 - a counter stage that inputs the control signal and generates a plurality of sequential signals to a plurality of transistors, wherein the plurality of transistors source current from a power supply.
- [c2] The apparatus of claim 1, wherein the counter stage sequentially disables the plurality of transistors to cause a gradual reduction in an amount of current sourced from the power supply.
- [c3] The apparatus of claim 2, wherein the counter stage enables the plurality of transistors when power consumption by the integrated circuit does not need to be reduced.
- [c4] The apparatus of claim 1, wherein the plurality of transistors are each one selected from the group consisting of a p-type transistor and a n-type transistor.
- [c5] A circuit for reducing a rate of current change of a microprocessor, comprising:
- a control stage that is connected to a power terminal and a ground terminal, wherein the control stage generates a control signal; and
 - a counter stage that inputs the control signal and a clock signal, wherein the counter stage generates a first signal to a gate terminal of a first transistor.

- [c6] The circuit of claim 5, wherein the first transistor has a terminal connected to power and another terminal connected to ground, and wherein the first transistor sources current from power to ground.
- [c7] The circuit of claim 5, wherein the counter stage generates a second signal to a gate terminal of a second transistor.
- [c8] The circuit of claim 7, wherein the second transistor has a terminal connected to power and another terminal connected to ground, and wherein the second transistor sources current from power to ground.
- [c9] The circuit of claim 5, wherein the counter stage generates a last signal to a gate terminal of a last transistor.
- [c10] The circuit of claim 9, wherein the last transistor has a terminal connected to power and another terminal connected to ground, and wherein the last transistor sources current from power to ground.